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Highly resonant controller for multimode piezoelectric shunt damping

S.O.R. Moheimani, A.J. Fleming and S. Behrens

A new controller structure for piezoelectric shunt damping is proposed. The controller has a highly resonant structure and is implemented digitally on a piezoelectric laminate structure. Experimental results are presented demonstrating the effectiveness of the controller in suppressing structural vibrations.

Introduction: Piezoelectric transducers are under investigation as actuators and sensors for vibration control in flexible structures. These materials strain when exposed to a voltage and conversely produce a voltage when strained [1]. For vibration control purposes, piezoelectric transducers are bonded to the body of the base structure using strong adhesive material.

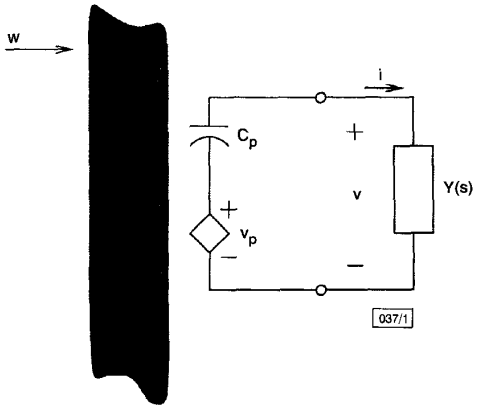

Fig. 1 *Electrical equivalent of shunted piezoelectric laminate*

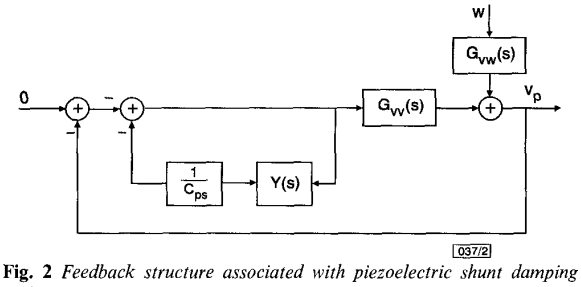

Fig. 2 *Feedback structure associated with piezoelectric shunt damping systems*

To suppress vibrations of the base structure, the piezoelectric transducer is shunted by an electrical impedance [2]. This impedance, particularly when implemented digitally, can be considered as a controller. The electrical equivalent of a shunted piezoelectric laminate structure is shown in Fig. 1. Here, w represents the external disturbance, while v_p is the voltage induced inside the piezoelectric transducer and is due to the mechanical strain in the base structure. The following equations describe dynamics of the composite system:

$$v_p(s) = G_{vw}(s)w(s) + G_{vv}(s)v(s) \quad (1)$$

$$i(s) = (v_p(s) - v(s))C_p s \quad (2)$$

$$i(s) = Y(s)v(s) \quad (3)$$

where C_p represents the capacitance of the piezoelectric transducer, $G_{vv}(s) = v_p(s)/v(s)$, $G_{vw}(s) = v_p(s)/w(s)$. Furthermore, the transfer function $G_{vv}(s)$ is typically found to be of the form

$$G_{vv}(s) = -\sum_{i=1}^{\infty} \frac{\gamma_i}{s^2 + 2\zeta_i\omega_i s + \omega_i^2} \quad (4)$$

where $\gamma_i > 0$ for $i = 1, 2, \ldots$.

From the above equations, the feedback structure of the problem can be identified as shown in Fig. 2. The real challenge is to find an effective structure for the controller (admittance transfer function), $Y(s)$.

Controller structure: We propose a controller with the following structure:

$$Y(s) = \frac{\sum_{i=1}^{N} \frac{\alpha_i\omega_i^2}{s^2+2d_i\omega_i s+\omega_i^2}}{1 - \sum_{i=1}^{N} \frac{\alpha_i\omega_i^2}{s^2+2d_i\omega_i s+\omega_i^2}} \cdot C_p s \quad (5)$$

where $\alpha_i > 0$, $d_i > 0$, $i = 1, 2, \ldots, N$ and $\Sigma_{i=1}^{N} \alpha_i = 1$.

This controller has two interesting properties: it is stable and stabilising, and has good robustness properties, i.e. the controller maintains closed loop stability in the presence of spill-over dynamics and incorrect model of the composite system. Furthermore, it is a strictly positive real system, i.e. it can be implemented as a passive system. However, for practical reasons, the controller has to be implemented digitally using the synthetic impedance circuit [3].

It can be observed that eqn. 5 has a highly resonant nature. It consists of a number of very narrow bandpass filters centred around those resonant frequencies that are to be suppressed. The only parameters in eqn. 5 that are to be fine tuned are d_1, d_2, ..., d_N. These parameters can be determined by solving an optimisation problem such as:

$$d_1^*, d_2^*, \ldots, d_N^* = \arg\min \|T_{v_p w}\|_2 \quad (6)$$

where $T_{v_p w}$ represents the closed loop transfer function from disturbance w to v_p.

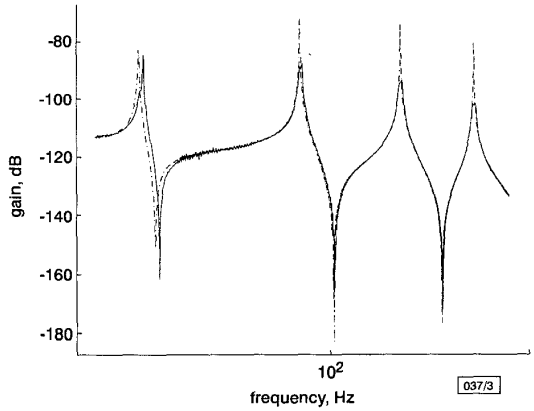

Fig. 3 *Open loop against closed loop experimental results*

- - - - open loop
——— closed loop

Experimental results: Experiments were performed in the Laboratory for Dynamics and Control of Smart Structures at the University of Newcastle, Australia. The experimental test bed was a simply-supported beam with a pair of identical colocated piezoelectric patches attached to either side. A voltage was applied to one of the patches to disturb the structure while the other patch was shunted by the synthetic impedance [3] implementation of eqn. 5. Displacement of the beam was measured at a point on its surface with and without the controller. The open loop and closed loop responses are compared in Fig. 3. It can be observed that some of the modes are heavily dampened (over 20 dB).

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S.O.R. Moheimani, A.J. Fleming and S. Behrens (*Department of Electrical and Computer Engineering, University of Newcastle, NSW, Australia*)

E-mail: reza@ee.newcastle.edu.au

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Skewing clock to decide races – double-edge-triggered flip-flop

P. Varma and K.N. Ramganesh

A clock-skew-based methodology for deciding races that are ordinarily settled by making feedback paths weak or resistive is proposed. Applying this to earlier work, a new static, double-edge-triggered flip-flop is derived that shows significant gains in terms of reduced power, increased frequency, and reduced gate area.

We propose a new technique for resolving a race between input and output nodes of latches and loops, wherein the latches and loops are enabled or disabled by a phase waveform such as the clock. The technique is based on the use of phase skew in deciding the race condition instead of, or in addition to, traditional methods such as weak/resistive paths for benefits such as reduced power consumption, and higher frequency response.

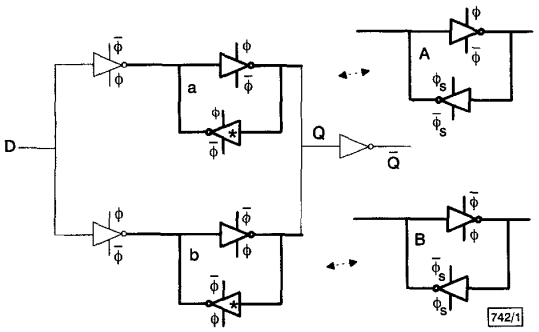

Fig. 1 *Schematic diagram of latches*

Fig. 1 highlights several latches in bold lines. Consider the latch labelled a in Fig. 1. The latch comprises a normal clocked inverter and a weak clocked inverter (marked by *). Both inverters are disabled by a high clock. The latch input is fed by the weak inverter output and the latch output (Q) is fed by the normal inverter output. When ϕ is high, the input and the output nodes of the latch can be set to identical values by the connecting circuits. Next when ϕ goes low, then both nodes are in a race to set each other. Output Q is compromised by the weak feedback. Thus an appropriately chosen weakness in feedback ensures that the input node always wins the race. Similarly, this method can be used in deciding races in other phased latches and loops also. We now describe a superior alternative for this method.

In latch a, consider skewing ϕ for the forward path relative to the backward path such that the backward path is enabled after a delay compared to the forward path. Thus the input node reaches the output through the forward path and sets it before the output gets a chance to do anything. There are two options that apply: (i) delaying the falling and rising clock edges equally; (ii) delaying the falling edge only, while keeping the rising edge unchanged. Cascading latches is complicated by option (i), because a delayed reverse path of one supposedly-disabled latch can contest the forward path of a preceding latch just when the preceding latch gets enabled. Option (ii) offers no such complications, but it is not as straightforward as option (i) to implement.

Next we apply the method described to a well-known, static, double-edge-triggered flip-flop by Gago *et al.* [1]. Fig. 1, excluding latches A and B, is a schematic representation of this flip-flop. Latches a and b are to be replaced by latches A and B, respectively, according to our clock skew method. The feedback paths of A and B use a skewed clock ϕ_s. Gago's flip-flop comprises six clocked inverters, three of which are enabled by a high ϕ and the rest are enabled by a low ϕ. Within each group of three clocked inverters, the clocked transistors are shared [1]. Thus Gago's flip-flop uses a total of $(4 + 2 + 2) \times 2 + 2 = 18$ transistors. Similar clocked transistor sharing in the flip-flop according to our method is reduced by the fact that two clocked inverters use unique skewed clock phases. However, since these two inverters take the same input (Q), they become free to share their Q-inverting transistors unlike [1] that loses this due to extensive clocked transistor sharing. Our circuit accordingly is shown in Fig. 2. The Figure also shows an amortised clocking arrangement, which is to be discussed later.

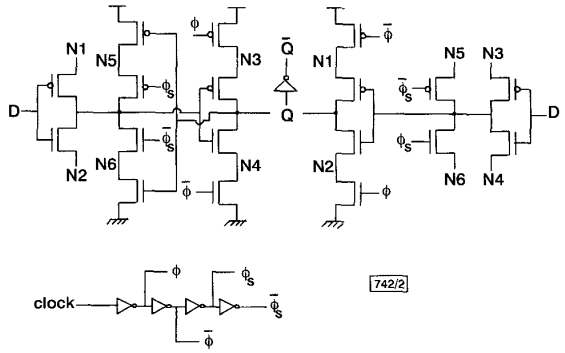

Fig. 2 *New DET FF and amortised clocking arrangement*

Gago's flip-flop does not work with minimum-area transistors and requires careful transistor sizing. The weak inverters are implemented using long-channel transistors and the clocked transistors are implemented using large-width transistors for driving the load of extensive sharing. By contrast, all transistors in Fig. 2 are implemented as simple, minimum area transistors ($W/L = 2.5$). We benchmark Gago and Fig. 2, using IBM PowerSPICE on MOSIS 0.25 µm N94S parameters. Gago's weak transistor ratios do not scale directly to this technology. Longer channels are necessary. W/L for the resistive transistors (M13, M14, M15, M16 in [1]) becomes 0.625 µm / 0.8 µm. Other ratios are taken from [1], namely 5 for transistors M5–M12 and 2.5 for the rest.

Table 1: Some comparisons

	Maximum frequency	Transistors	Area of gates
Gago *et al.*	3.076 Gbit/s	18	5.4375 µm²
Ours	5.264 Gbit/s	20	3.125 µm²

The performance of our circuit vis-à-vis Gago is given in Table 1. While Gago's method saves two transistors by extensive sharing, the simplicity of our transistors results in a substantial reduction of the total gate area. Since all transistors are switched, this implies a substantial reduction in switching capacitance. Next, given that there are no slow, resistive transistors involved in our circuit and no slowdown due to one inverter trying to overcome another simultaneously-ON inverter, the superior speed of our circuit in Table 1 comes as no surprise. The speed was obtained by observing a toggling flip-flop wherein ~Q was connected back to D. The waveform of our flip-flop at its maximum frequency is shown in Fig. 3. The maximum frequency does not change if a locally-generated ϕ_s is used. One method to improve Gago's speed may be to use Blair's method [2] for improving Hossain's static flip-flop [3]. Blair reduces switching capacitance by substituting each weak, switched transistor by a series combination of an